

Abstract of the Disclosure

Phase locked loops (PLL) providing for conditional holdover are especially suited for use in communications networks. During a holdover condition, the timing signal is generated without use of an input reference clock signal. The PLLs may either enter or remain in a holdover condition if the demonstrated or expected quality level of the output of the PLL equals or exceeds the indicated quality level of the input reference clock signal. In this manner, the timing signal has an expected quality level equal to or greater than the quality level of the reference clock signal. Accordingly, network timing errors may be reduced to levels below those associated with using the reference clock signal.